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Claims

[c1] What is claimed is:

1. A method for fabricating a semiconductor transistor device having ultra-shallow source/drain extensions, comprising:

preparing a substrate;

forming a gate structure on said substrate, the gate structure having sidewalls and a top surface;

forming an offset spacer on each said sidewall of said gate structure;

ion implanting said substrate next to said gate structure to form shallow-junction doping regions;

depositing a spacer liner on said offset spacer and on said top surface of said gate structure;

depositing a spacer layer on said spacer liner;

performing a stress modification implantation process to alter said spacer layer from a tensile status to a less tensile status, or into a compressive status; and

dry etching said spacer layer to form spacers.

[c2] 2. The method according to claim 1 wherein said substrate is a silicon substrate.

[c3] 3. The method according to claim 1 wherein said gate

structure is a poly gate structure.

[c4] 4. The method according to claim 1 wherein a gate dielectric is interposed between said gate structure and said substrate.

[c5] 5. The method according to claim 1 wherein said spacer layer is made of silicon nitride.

[c6] 6. The method according to claim 1 wherein said stress modification implantation process uses germanium or xenon as dopants.

[c7] 7. The method according to claim 1 wherein said stress modification implantation process uses dopant species, which are electrically neutral.

[c8] 8. The method according to claim 1 wherein said stress modification implantation process is carried out in an energy range of about 25 to 150KeV.

[c9] 9. The method according to claim 1 wherein said stress modification implantation process is carried out using germanium as a dopant at an implant energy of about 100 KeV and an implant dose of about 5E15atoms/cm^2.

[c10] 10. The method according to claim 1 wherein said shallow-junction doping regions are P type doped.

[c11] 11. A method for fabricating a semiconductor transistor device, comprising:
providing a silicon substrate;
forming a gate structure on said silicon substrate, the gate structure having sidewalls and a top surface;
forming an offset spacer on each said sidewall of said gate structure;
performing a first ion implantation to implant said silicon substrate next to said gate structure so as to form first doping regions acting as a source/drain extensions of said semiconductor transistor device;
depositing a spacer liner on said offset spacer, on said top surface of said gate structure, and on said first doping regions;
depositing a spacer layer on said spacer liner;
performing a stress modification implantation process to alter said spacer layer from a tensile status to a less tensile status, or into a compressive status;
dry etching said spacer layer to form spacers; and
performing a second ion implantation to implant said silicon substrate next to said spacer so as to form second doping regions acting as a source/drain of said semiconductor transistor device.

[c12] 12. The method according to claim 11 wherein said stress modification implantation process uses dopant

species, which are electrically neutral.

[c13] 13. The method according to claim 11 wherein said stress modification implantation process uses germanium or xenon as dopants.

[c14] 14. The method according to claim 11 wherein said stress modification implantation process is carried out in an energy range of about 25 to 150KeV.

[c15] 15. The method according to claim 11 wherein said stress modification implantation process is carried out using germanium as a dopant, at an implant energy of about 100 KeV and an implant dose of about 5E15atoms/cm^2.

[c16] 16. The method according to claim 11 wherein said stress modification implantation process has a projected range (Rp) that is smaller than said spacer layer's thickness.

[c17] 17. The method according to claim 16 wherein said spacer layers thickness is about 600~700 angstroms.

[c18] 18. The method according to claim 11 wherein said spacer layer is made of silicon nitride.

[c19] 19. The method according to claim 11 wherein a gate dielectric is interposed between said gate structure and

said substrate.

[c20] 20. The method according to claim 11 wherein said stress modification implantation process reduces vacancy defects of said silicon substrate.